Hybrid Modules as an Alternative to Paralleled Discrete Devices
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Abstract
Mosfets are currently being used in an increasing number of applications, especially battery powered and high frequency systems. In many of these systems several chips must be paralleled to achieve the necessary performance. The chips can either be paralleled as discrete plastic packages, or as chips within a hybrid module.

Hybrid modules have the advantage over paralleled discrete devices when more than 5 chips in parallel are required to develop a design. In this type of system the hybrid module will be the smallest, electrically isolating the module will be easiest, thermal management will be the best, and the total system cost will be the lowest.

Paralleled discrete devices have the advantage over hybrid modules when only 2 or 3 chips in parallel are required to develop a design. In this type of a system, discrete devices paralleled on a PCB provide the smallest footprint. Also electrical isolation and parasitic inductance are usually not difficult to manage in this size system.

Several applications, and their implementations as parallel discrete devices on a PCB and as hybrid modules, are discussed and used to illustrate the tradeoffs between solutions.

Background – Paralleling Mosfets
Reduction of mosfet RDS ON has generated electronic applications which were not previously feasible. Many of these applications require even lower RDS ON than is available with a single mosfet chip.

Fortunately mosfet chips are relatively easy to parallel. This is due to the positive coefficient of on state resistance. If two mosfets are conducting in parallel, and one has a lower on state resistance than the other, the lower resistance device will at first carry a larger share of the current. This larger share of current will generate more heat in the device. The temperate of the device then rises; increasing the device's on-state resistance and forcing more current to the other device. In this way, the positive coefficient of on-state resistance forces paralleled mosfets to share current. No external circuits as emitter resistors as used when paralleling bipolar devices are required to ensure mosfet sharing during conduction.

Although the positive coefficient of on state resistance stabilizes and equalizes paralleled mosfet chips during conduction, it does not control the sharing of current when the device is in the active region, turning on or off. During this switching time, the current in each device is determined by the transfer characteristics of the chips. To insure sharing of current during switching, the transfer characteristics of the chips to be paralleled should be matched. This is most commonly done by simply paralleling identical part numbers without any other matching schemes. However, it can be better accomplished by matching devices according to Vgs threshold, using devices from only one diffusion lot, or by using adjacent chips from a wafer.

The choice of matching techniques depends primarily upon the importance to the end application of good current sharing during switching. For example, in an induction heating system operating at 200,000 Hertz, the
switching characteristics are much more important than in an on-off DC motor control.

Assuming the transfer characteristics of the mosfets are sufficiently matched for the application, current will be shared by the chips during the switching interval. However, this assumes the gate source voltage of each of the paralleled chips is the same during this time. Unfortunately the gates of the mosfets cannot simply be tied together. A small resistance or ferrite bead must be used in the gate lead of each mosfet. Without the resistor or ferrite bead, the large capacitance of the mosfet gate, coupled with the usually small stray parasitic inductances of the circuit can cause unwanted high frequency oscillations. Careful physical layout of the paralleled mosfet circuit is required to reduce the stray inductances and the associated unwanted oscillations.

In addition to the on state characteristics and switching characteristics of paralleled mosfets, attention must be paid to the body diode of the device if it is to be used as a free wheel diode. In many applications, particularly motor control, the body diode of the mosfet is used as a free wheeling diode. Although the channel of the mosfet has a positive temperature coefficient that causes the on current to be shared equally among several chips, the body diode of the mosfet typically has a negative temperature coefficient. For example, if two diodes with negative temperature coefficients are paralleled, and one has a slightly lower conducting voltage than the other, it will carry a larger share of current. Further, since it carries a larger share of current, it will generate more heat and increase in temperature. Since its conduction voltage decreases with increasing temperature, the increase in temperature will cause the chip which is already carrying a larger share of current to carry an even larger share of current. Thus the negative temperature coefficient of the diode will magnify current imbalances.

If free wheel diode characteristics are critical to an application, the diode characteristics can be matched similarly to how mosfet characteristics can be matched. The diode’s conduction voltage can be matched, chips from only one diffusion lot can be used, or adjacent chips from a single wafer can be used. In addition to these techniques, careful physical layout of the circuit is even more critical to insuring current sharing during body diode conduction. Because of the negative temperature coefficient of body diode conduction voltage, care must be taken to insure that the chips stay at nearly the same temperature. This equalization of temperature is achieved by positioning the parts close together, and mounting them on a common heat sink or conducting pad. Often this will be an extra copper buss on a printed circuit board or a mutually conducting thick copper (0.30 mm) pad in a hybrid module.

Two Techniques — Hybrid Modules and Paralleled Discrete Mosfets

There are two techniques to achieve a power mosfet circuit which requires an RDSon lower than is readily available in a single silicon chip. The first technique is to parallel several chips on a printed circuit board. This is a simple straightforward method of selecting a suitable device (typically a TO-220, TO-267, or TO-3P plastic package) and laying out a printed circuit board to accommodate the devices. Using this technique, a board must be designed properly, with consideration paid to gate resistors, symmetry of the physical layout to reduce parasitic inductance, and consideration to equalizing temperature.

This design can usually be done easily when only two or three devices need to be paralleled for each switch. In this case it is typically easy to create a layout which minimizes stray inductance, and the devices can easily be mounted to readily available commercial heat sinks or to custom insulated metal substrates which will equalize the temperature of the devices. However, if good matching is required, the only technique available to match devices is the testing of device characteristics. It is typically impossible to verify diffusion lot or wafer location in discrete plastic packages such as the TO-220, TO-3P or TO-267.

The second technique is to use a hybrid mosfet module. These modules parallel the mosfet chips at the silicon level. This allows the chips along with their gate resistors to be placed very closely together. The tight spacing functions in reducing the parasitic inductance between chips, as well as assuring uniform temperature distribution across from chip to chip.

A cross section of a typical mosfet module is shown in figure 1. In this diagram, a silicon
A mosfet chip is mounted via solder to a layer of thick copper which is directly bonded to a ceramic substrate. The other side of the substrate is also directly bonded to a layer of thick copper. This copper is mounted to a copper base plate via solder. In this construction the first copper layer serves as a conduction path for the drain current of the mosfet. In addition it is also a thermal spreading layer for the heat generated in the chip. This spreading layer serves to keep the paralleled mosfet chips at the same temperature, insuring good on-state sharing, as well as good diode conduction sharing.

The ceramic substrate provides electrical isolation while conducting heat away from the chip. In a hybrid module the isolating ceramic layer can either be made of Alumina, Aluminum Nitride or Beryllium Oxide. These materials have thermal conductivities of 35 Watts per meter Kelvin (W/mK), 170 W/mK, or 210 W/mK respectively. Typically these materials provide isolation voltages up to 6000V using a 0.30 mm thick layer. In this configuration the thermal performance for a given isolation voltage is much better than isolating thermal pads, giving the hybrid module a significant advantage in its ability to dissipate heat.

**Application 1 – 100V, 800A Three Phase Full Wave Inverter for a 28V Bus.**

The first case study to compare hybrid mosfet modules to paralleled discrete devices is a three phase full wave inverter bridge for 28V buss. A simplified schematic of this circuit is shown in figure 2. It is essentially a standard 3 phase inverter for driving AC brushless motors, and is used to control turret rotation in a military gun system.

In this application, controlling the total amount of heat generated by the inverter was critical, because the overall system was limited in the amount of heat it could dissipate. To reduce the total heat, a very low target RDSon of 1.55 milli-Ohms at 25°C was selected. This necessitated paralleling eight 100A 100V mosfet chips for each switch.

The circuit was prototyped using discrete plastic SOT-227 devices, which is a small isolated hybrid module. One leg of the inverter includes two mosfet switches connected in series. Each leg was constructed using 8 SOT-227 packaged devices. This provided a test bed for the circuit, but was viewed as unfeasible for production because a full implementation of the three phase bridge would require 24 such devices. Each of the 24 devices would require 2 mounting screws and 4 electrical interconnect screws. The total assembly would require 144 screws, all aligned and torqued to specification.
The production design for this project utilized a custom designed hybrid module. The device, shown in Figure 3, implemented a single leg of the inverter. Three of the modules would be required to implement the assembly. In this design each module required four mounting screws and three power connection screws. The full assembly required only 21 screws.

This project showed mechanical design and layout of the system to be critical to the electrical performance. The paralleled SOT-227 prototype showed a significant ring-up voltage due to the parasitic inductance of the circuit. This led to the specification of extra capacitors to be distributed along the DC buss. When the production custom hybrid module was tested, it was found that the parasitic inductance and associated ring-up had been reduced enough to eliminate all of the extra capacitors which the SOT-227 prototype required.

In addition, the custom hybrid device also proved to be a smaller, denser packaging solution. The SOT-227 based inverter required a total mounting area of 235cm². The custom hybrid module based inverter has a total mounting area of 188 cm². This represents a 20% reduction of heat sink mounting area.

Application 2 – 900V, 400A Single Mosfet for Induction Heating.

This application is for a very large mosfet module to be used in an amplifier for induction heating. The main design considerations in this application are providing a low RDSon switch, insuring good sharing during switching, and providing 2500V isolation between the device and heat sink while managing heat flow.

The hybrid device shown in Figure 4 consists of thirty-six 14A, 900V mosfet chips paralleled to form a single mosfet switch. The total RDSon of this aggregate switch is 24 milli-Ohms at 25°C. Each of the chips is typically packaged in a TO-3P and has a maximum RDSon of 0.85 Ohms in the discrete version.

To assure good sharing during switching each mosfet has a gate resistor mounted on a common gate bus. In addition the layout is symmetrical around the source and drain leads of the overall switch. To assure the devices are at similar temperatures, and to efficiently dissipate the heat they generate, the isolating ceramic was chosen to be aluminum nitride with copper directly bonded to it. This material rapidly conducts heat away from the chips to the copper base plate. The large thermal mass of the copper base plate combined with copper’s very high thermal conductivity of 390W/mK help keep the module a consistent temperature across the entire base plate, thus assuring the chips are uniform in temperature.

The aluminum nitride layer also serves as electrical isolation in addition to thermal management. In a high voltage mosfet switch such as this one, there must be significant electrical isolation between the electrical terminals of the device and the heat sinking base plate. Isolation requirements in excess of 2500 V_{RMS} are not uncommon. This application required 3000 V_{RMS}.

Application 3 – 100V, 420A Mosfet Single Phase Full Wave Bridge for Telecommunications DC-DC Converter

In this application four mosfet switches are required to create a single-phase AC inverter.
The inverter is used to generate a high frequency (40 – 50 KHz) sinusoidal current. The current is then fed through a transformer to increase or decrease the output voltage. By using a high frequency AC signal, the transformer can be much smaller and more efficient than would be required if a line frequency (60 Hz) AC was used. Figure 5 shows a simplified schematic for a single-phase inverter.

![Figure 5 – Simplified Schematic of a Single-Phase Inverter](image)

In this application, the most stringent requirement is cost rather than performance. Adequate performance can be achieved from paralleling discrete devices or from a hybrid module.

Each of the switches has a total maximum RDSon of 3.3 milli-Ohms at 25°C, and is constructed of six 70A, 100V mosfets. Each mosfet also has a six ohm gate resistor. The discrete solution is created by paralleling 6 TO-3P packages on a printed circuit board or insulated metal substrate. The Hybrid solution, as shown in Figure 6, is created by paralleling the silicon from these same packages on a ceramic substrate with a copper base plate. Each hybrid module contains two switches to create half of the single phase full wave bridge.

To properly evaluate the cost comparison between the discrete solution and the hybrid solution, one must include not just the silicon costs but also the costs of the labor to assemble the system, as well as the associated heat sinks and isolating thermal pads. In this system, 6 mosfet chips in TO-3P packages, 6 heat sinks, 6 isolating pads, and 6 sets of mounting hardware are required for each switch. A module solution would require only 1 heat sink which could be shared with other components, no isolating pads, and only one set of mounting hardware. A reduction in part count can often be a large advantage in reducing overall system costs.

The biggest disadvantage to hybrid module use is the lack of standards for form, fit, and function. This implies that each hybrid device is a custom device for a particular application or user. In many situations the device will be only built by one source. For most applications, developing identical “custom” hybrid devices at multiple vendors is cost prohibitive. Thus, the hybrid solution is a sole source solution.

### Application 4 – 250V 720A Single Mosfet With Series Diode for Welding DC-DC Converter

This application is essentially a large Buck converter. The power components consist of a mosfet switch in series with a fast recovery diode, as schematically shown in Figure 7. In this application the large current required was satisfied by paralleling several hybrid modules. Each of the hybrid modules contained six 40A mosfet chips and 6 high speed diode chips. Three of these devices were paralleled to create one very large device. The Hybrid device is shown in Figure 8.

In this situation, a completely discrete paralleled device would have required 36 paralleled discrete devices. This hybrid solution could have been built as one module, but was implemented as three devices to create economies of scale. One part could be used to
build 240A, 480A, or 720A circuits. Had the part been scaled to use one device for the 720A circuit, a separate device would have to be designed to build a 480A circuit, and still a third device to build the 240A circuit.

Summary

Mosfet characteristics are well suited to paralleling several devices to achieve lower RDSon values and higher currents. As more mosfet chips are paralleled, a hybrid solution can be more attractive than paralleling discrete plastic packages such TO-220, TO-267, or TO-3P. In terms of performance the hybrid solution can have lower parasitic inductance due to the parts being arranged more closely. Electrical isolation of the circuit from the heat sink is usually handled inside a hybrid device through the use of ceramics. In a discrete solution isolating electrical signals must be done through the use of thermally conductive isolating pads. A hybrid module is typically much easier to mount and use than discretes. When the costs of labor, mounting hardware, and circuit area are included in the equation, the module is often a more attractive implementation of a circuit. If a lower RDSon is necessary, several hybrid modules may be paralleled to achieve circuits which would require a great number of discrete devices. The comparison between modules and discrete devices is summarized in Table 1.

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Table 1 – Comparison of Hybrid and Discrete Paralleling Techniques

References

3. “Motorola TMOS Power Mosfet Transistor Device Data”, Motorola, 1995