Electro-Thermal Modeling of Multi-Megawatt Power Electronic Applications Using PSPICE™

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Abstract:-- ***Circuit modeling is an essential tool in the design of multi-megawatt power electronic applications. Specifically, for circuits using SCRs and Diodes, both the on-state forward voltage drop and transient thermal impedance are complex characteristics, for which, only recently have adequate mathematical models been developed. The on-state forward voltage drop can be modeled by both the classical ABCD and the new MNOPQ... parameters. The transient thermal impedance can be well represented via four or five exponential terms representing the significant transient thermal time constants of the device. There is, however, one complication which is not represented in the ABCD & MNOPQ... models. This is the dependence of the on-state voltage on the instantaneous junction temperature. This affect, termed COD or VFIT, requires that the model be Electro-Thermal, meaning that this important dependence must be accounted for in a microsecond by microsecond manner during the simulation.***

This paper describes the basic device modeling equations and the techniques required to use these models in "analog" simulation programs such as PSPICE™. Parameter extraction from empirical test data is described and the electro-thermal model accuracy evaluated. The final and new result is an electro-thermal model for power electronic application using SCRs and Diodes which includes the dynamic affect of instantaneous junction temperature on the on-state voltage. The resulting PSPICE™ electro-thermal model is expected to be an important design tool in multi-megawatt power electronic applications, providing the detailed analysis the power electronic engineer needs to quickly evaluate an existing or proposed power electronic application.

I. INTRODUCTION

Circuit modeling is an important tool in the design and development of power electronic applications. Specifically, for circuits using SCRs and diodes, both the on-state forward voltage drop and transient thermal impedance are complex characteristics. Only recently have the authors[1-4] and others[7,9] developed adequate mathematical models for these fundamental characteristics. The expanded use of these models, however, depends upon: 1. The understanding of how to use these models, 2. The trade-off of the accuracy vs. simplicity of the models, and 3. The availability of sufficient parametric data (modeling coefficients) for devices. The main substance of this paper is how to use the "analog" circuit simulator software such as PSPICE™ in combination with the device modeling equations, including the dynamic dependence of the on-state voltage with the instantaneous junction temperature. The importance of this temperature dependence, termed VFIT[**V**$_{tm}$ as a **F**unction of **I**$_{tm}$ and junction **T**emperature [2] or COD **C**oefficient **o**f **D**ependence [7], has been described in the literature. The resulting electro-thermal model is expected to be an important design tool in multi-megawatt power electronic applications.

Previous papers by the authors [1-4] and others[7-9,11,12,15] have addressed the mathematical modeling of SCRs and diodes. As has been described, the forward on-state forward voltage drop can be modeled by both the classical ABCD and the new MNOP... parameters. The transient thermal impedance has been shown to be well represented via four or five exponential terms representing the significant transient thermal time constants of the device. The methodology to quickly and accurately calculate the forward voltage drop and transient thermal impedance modeling parameters has been discussed and described in detail [1-4].

There is, however, one complication which is not represented in the ABCD & MNOPQ... models. This is the dependence of the on-state voltage on the instantaneous junction temperature. This affect, termed COD[7] or VFIT[2] requires that the model be electro-thermal. This permits the important dependence of the on-state voltage with the instantaneous junction temperature to be accounted for in a microsecond by microsecond manner during the simulation.

This paper will describe the basic device modeling equations and the techniques required to use the "analog" simulation program PSPICE™ to simulate a given power electronic application. Parameter extraction will be made on empirical test data and the electro-thermal model accuracy will be evaluated.

The final and new result is an electro-thermal model for power electronic application using SCRs and diodes which include the dynamic affect of instantaneous junction temperature on the on-state voltage. This information is considered to be an important step in providing a tool for power electronic design engineers to quickly evaluate a proposed or existing power electronic application.

IIII. PSPICE™ SCR (Diode) NON-VFIT MODELING

Next we will describe how the SCR(Diode) model parameters can be used in the "Analog" simulation computer program such as PSPICE™.

A. PSPICE™ Model Electrical Circuit:

The PSPICE™ electrical-thermal analog circuit of an SCR is diagramed in Figure 3. The circuit consists of a sinusoidal source, a load resistor R_L and the SCR V_{tm} model which is connected A to K. The SCR model consists of a Diode (D_scr), a voltage controlled voltage source (E_Vtm), and a zero voltage source current sensor (V_Pwr_Sen). The SCR current is: Itm = I(V_Pwr_Sen). The SCR electrical model provides the correct instantaneous on-state forward voltage drop for any value of instantaneous anode current. This is achieved by sensing the anode current I*(V_Pwr_Sen) and using the ABCD or MNOPQ.. V_{tm} models to force the correct instantaneous Vtm by the Value statement in (E_V_{tm}). This is illustrated by the circuit in Figure 3. This circuit was first presented in Reference [1] and does not include the temperature dependence of the on-state forward voltage drop. Note the ABCD and MNOPQ... V_{tm} Model equations are given in the upper right corner of Figure 3. and describe a non electro-thermal model of SCRs and Diodes. The Net List Code Fragment 1 of the PSPICE™ SCR model is shown in detail in the Appendix. Note in the listing an asterisk at the beginning of the line makes that line a comment, i.e., the V_{tm} ABCD Model is active and the MNOPQ... model is disabled for this case. The thermal circuit has five stages where the values of the analog components are determined from a regression of the transient thermal impedance as described in Reference [4]. All of the parameter values for A, B, M, N, ... R_n, TAU_n $Cn=TAU_n/R_n$ are inserted via PSPICE™ Parameter Statements as noted by the curly brackets around the label e.g., {A}.. This non-electro-thermal model is useful in applications which do not have extreme junction temperature swings such as steady state ratings.

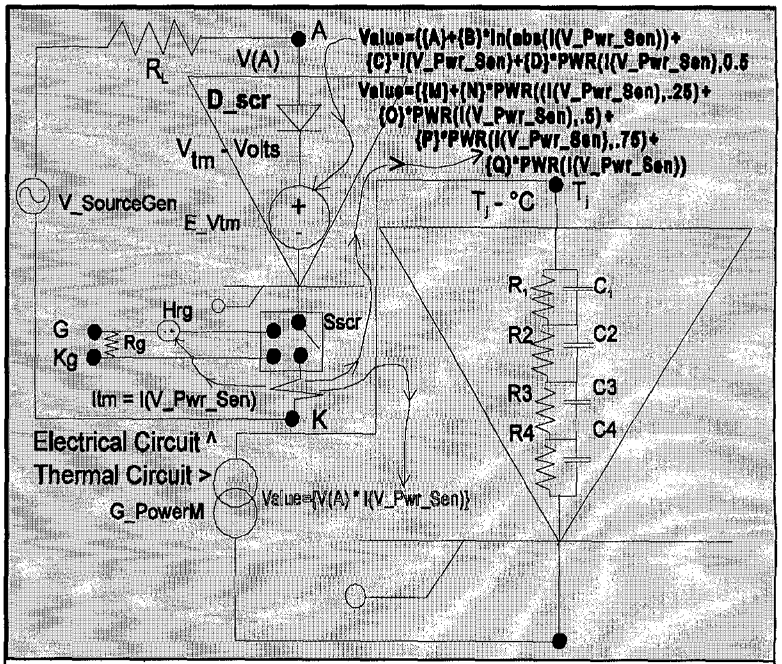

Figure 3. Diagram for Implementing ABCD or MNOPQ.. Vtm Models into PSPICE

B. PSPICE™ Model Thermal "Circuit"

The thermal circuit is also diagramed in Figure 3. It consists of a voltage controlled current source (G_PowerM). The value of this current source (which represents power dissipation in the device) is controlled by the calculated instantaneous power dissipation in the SCR i.e., V(A) * I*(V_Pwr_Sen). The current source then drives the analog electrical to thermal equivalent circuit for the device i.e., four or five sections of R-C parallel stages. This is the simplified transient thermal impedance model of the SCR or diode.

The Net List for this model is also provided in the Appendix, Code Fragment 1, where R1,C1 connect from the Tj Node via Tj1 to R2,C2 etc. and the voltage at the node Tj represents the virtual junction temperature rise for any power dissipation waveform and is, by definition, the transient thermal impedance for a unit step of power dissipation.

The Net List for the SCR model used to generate the data in this plot is presented in the Appendix. Note the terminals of the model are defined in the .SUBCIRCUIT The actual test circuit is not included in the net list but would be inserted into the circuit as a XSA component using the PRX_TBK7 Model

C. PSPICE™ ABCD or MNOPQ... Non-Electro-Thermal Waveforms

The PSPICE™ waveforms for the Powerex T9G0 withstanding a 17,000-Ampere single cycle surge are illustrated in Figure 4. This figure is from Reference [1]. Note that not only is the current waveshape through the SCR, I(Rload) displayed but also the Forward Voltage Drop, V_{tm} , Power Dissipation, Pt and the resulting Virtual Junction Temperature Waveforms. The power dissipation

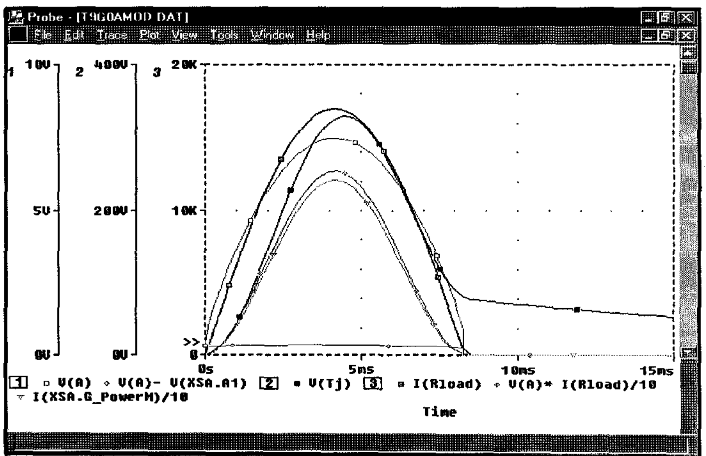

Figure 4. ***POWEREX*** T9G0A SCR PSPICE™ Waverforms

II. TRANSIENT THERMAL IMPEDANCE MODELS

There are two fundamental thermal-electrical analog models which describe the transient thermal response of power SCRs and diodes. First there is the physical ladder model and second the simplified(with regard to solving the transient differential equations) model. This model, while losing the interior physical temperature points, has the same external transient response as will be demonstrated in Figures 1. and 2. The transient thermal response is often incorrectly referred to as transient thermal impedance [11,16].

A. SCR and Diode Physical Ladder Model

Figure 1. provides an example of the Transient Thermal Response Physical "Ladder" Model. The electrical - thermal analog PSPICE™ circuit is displayed along with the PSPICE™ v(T_j) transient response for a step function input of one Watt, (actually represented by 1 Amp. In the analog model). This is the transient junction temperature response which, by definition [16], is the transient thermal impedance of the device. The ladder model is a result of carefully analyzing the thermal resistance and thermal capacitance of each physical **layer** of the SCR or diode. The classical thermal - electrical analog permits the electrical engineer to calculate the thermal resistance and thermal capacitance of each of the layers in the device. This is automatically calculated in STARS(Standard Thyristor Application Ratings) ThZDev program as described in reference [3]. The result is the ladder circuit as included in Figure 1. The transient thermal response can then be evaluated in PSPICE™ from this thermal analog circuit as described in [3]. The ladder network ,however, is too complex to be used as a circuit model but can be simplified with good accuracy by regression of the resulting transient thermal response curve into four or five series connected parallel RC stages [2] as will be described next.

B. SCR and Diode Simplified Model

Figure 2. is the Simplified Transient Thermal Impedance Model. This is also an electrical-thermal analog circuit, in which is the series connection of N parallel RC stages as illustrated by the PSPICE™ insert circuit diagram (Note; N=5 in this example). The values of the components are established by regression of the transient thermal response curve just described. The resulting PSPICE™ transient response of this circuit is given in Figure 2. This is the transient thermal response V(T_j) waveform. Note that the transient temperature waveforms of Figures 1 and 2 are virtually identical (deviating less than 0.1% over the full time range) as required by the claim that the two models are identical. While the simplified model loses most of the spatial temperature relationships [3], that is, the temperatures of given physical locations in the device, it provides a simplified overall transient solution of junction temperature and can readily be implemented in hard code simulation [1].

C. SCR and Diode On-State Voltage Model

The ABCD and MNOPQ... model parameters are described in References [1], [2] and [3] along with the methods to extract the parameters. As implemented In the STAR (Standard Thyristor Applications Ratings) program by

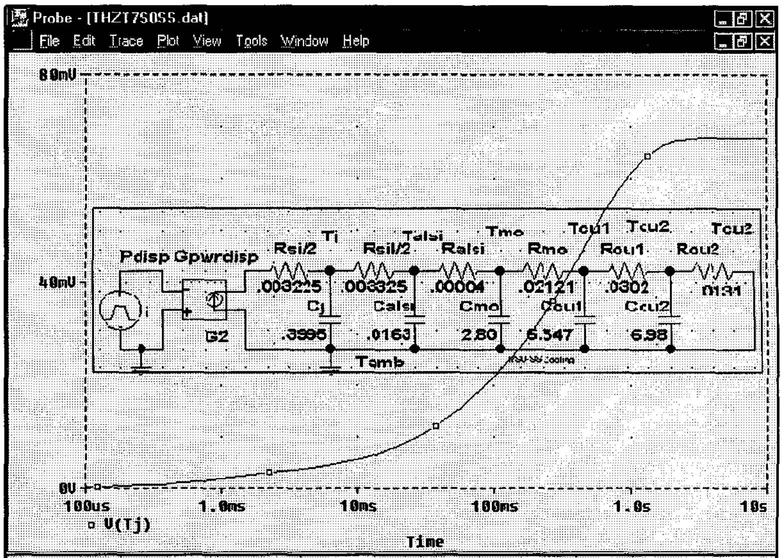

Figure 1. The Transient Thermal Impedance Physical "Ladder" Model Equivalent Circuit is illustrated in this PSPICE Diagram and T_j Transient Response Waveform.

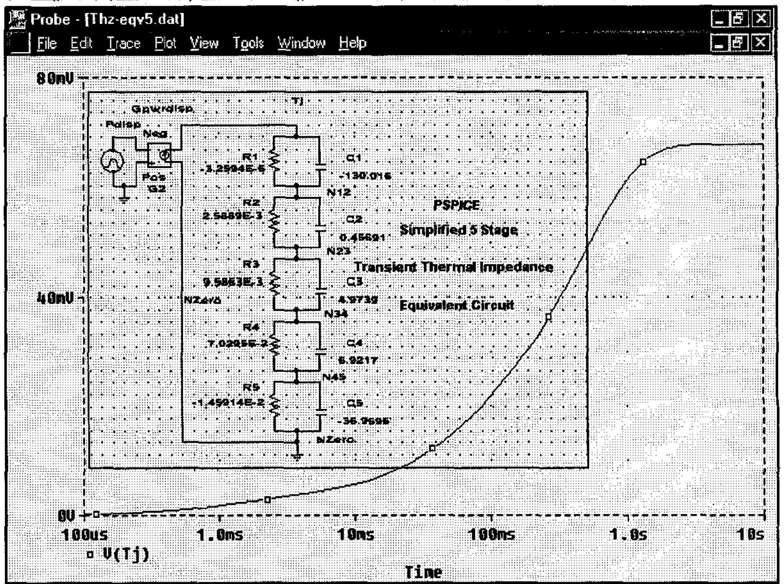

Figure 2. The "Simplified" Transient Thermal Impedance Model is a Series Connection of N Parallel RC Stages as displayed in the PSPICE Diagram and Waveform

menu selecting; Data, Vf-Vtm Model Parameters, the range of anode current, and then ABCD or MNOPQ... The parameters, for the chosen device, are quickly evaluated from the classical (5 points per decade) on-state forward voltage drop tables. and placed into a parameter file.

is displayed as a *current* where (1 Amp = 1 Watt). Temperature is shown as the analog voltage V_{Tj} (1 Volt=1°C) at the circiuit node T_j. The peak junction temperature is 356°C at 4.25msec which was demonstrated [1] to be in good agreement with other methods of calculating the junction temperature. The SCR Electrical Model provides the correct (Non-Isometric) instantaneous on-state forward voltage drop for any value of instantaneous anode current. This is achieved by sensing the anode current I*(V_Pwr_Sen) and using the ABCD or MNOPQ... V_{tm} Models to force the correct instantaneous Vtm by the Value statement in (E_Vtm). This is illustrated by the circuit in Figure 3. and the Net List Code Fragment 1 in the Appendix.

IV. PSPICE™ MODEL INCLUDING the TEMPERATURE DEPENDENCE of the ON-STATE FORWARD VOLTAGE DROP

The PSPICE™ model for the SCR or diode is again diagrammed in Figure 5, but now includes VFIT. The net list for Figure 5. is presented in Code Fragment 2 in the Appendix, The SCR(diode) is implemented as a Sub-circuit in PSPICE™. The thermal circuit again has five stages where the values of the analog components are established from a regression of the transient thermal impedance. Parameter values for the VFIT equation and R_n, TAU_n $Cn=TAU_n/R_n$ are inserted via PSPICE™ parameter statements.

V. PLOTS of ON-STATE VOLTAGE INCLUDING COD or VFIT

The On-StateVFIT VI curves from a previous paper [2] by the authors will now be compared to the VFIT VI curves of the new electro-thermal PSPICE™ SCR(diode) model for the 4500V, 77mm diameter C784/TBK7 SCR.

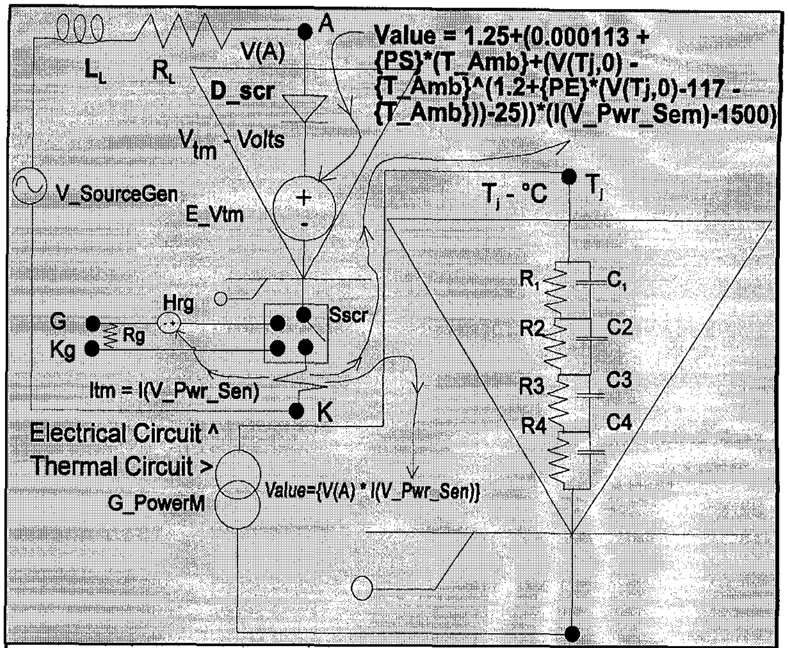

Figure 5. Diagram for Implementing VFIT Model into PSPICE

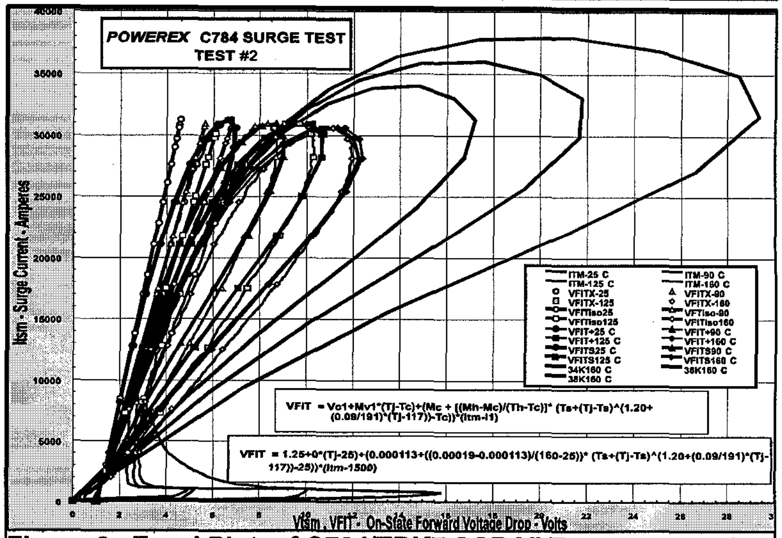

Figure 6. Excel Plot of C784/TBK7 SCR VI Traces created by VFIT and STARS Arbitrary Waveform Module

A. On-State Voltage including COD or VFIT

Figure 6. is a plot of On-State Voltage including COD or VFIT Using the STARS, Visual Basic, Arbitrary Current Waveform, Visual BASIC, Program [2] and Excel to plot the results. This plot is from Reference [2] on Isothermal surge and overloads of SCRs and Diodes and did not use PSPICE™.

B. The On-State Voltage including COD or VFIT and PSPICE™

The On-State Voltage including the COD or VFIT using PSPICE™ is illustrated by the VI loops in Figure 7 for the C784/TBK7 SCR. This is data plotted from the new PSPICE™ Electro-Thermal Model. Note the uneven spacing of the data points (curve markers) as PSPICE™ changes the time step to make sure the *process in converging to the correct solution.* The characteristic parrot beak VI traces observed just prior to device failure in empirical testing indicates the Electro-Thermal PSPICE™ model is working. The fact that Figure 7. reaches 30 Volts VTM at 37,000A instead of 38,000A is due to the sub-microsecond step PSPICE™ is taking versus the 500 microsecond steps in the much less automated procedure of using Visual BASIC in the Arbitrary Waveform Module of STARS and Microsoft Excel in Figure 6.

VI. EMPRICAL TESTING, VFIT PARAMETER EXTRACTION and EXAMPLE WAVEFORMS

The VFIT Equation is described in detail in Reference [2]. The equation is based on the SCR and diodes at higher anode currents where the on-state voltage isothermal curves can be assumed to be approximately linear. Additional assumptions; include the on-state voltage at low current varies linearly with junction temperature (usually negative), the slope of the on state voltage varies linearly with current in the low to moderate current densities and increases with a positive exponent at high to extremely high currents (typically 1.1). While the constant exponent provides a good model for high anode currents, extremely high surge currents require a increasing exponent with junction temperatures (example 1.1 to 1.25) to model the non-repetitive surge currents as illustrated in Figure 8 for a 3500V, 33mm diameter general purpose diode.

Figure 8. includes the VFIT model VI traces which match the empirical test data at 40, 90,150, and 180°C. In addition, at 180°C VFIT calculated VI surge current curves of 8900 and 9,400 peak Amperes extend the surge current levels to include the destructive region of the diode.

Again, as in Reference 2, the characteristic "parrot beak" is observed (note that the axis have been switched to the correct independent variable which is anode current). The "parrot beak" is a characteristic which has been observed in empirical testing just prior to device failure [7].

The agreement between the empirical data and the VFIT generated VI plots is good. Note that PSPICE™ also provides the instantaneous power dissipation and junction temperature waveforms during the surge current, as will be shown in Figure 9.

The "parrot beak" characteristic started at 8900A peak surge current with a case temperature of 180°C. The resulting simulated peak junction temperature was 637°C. The device failed at 9000A when the case temperature was increased to 200°C.

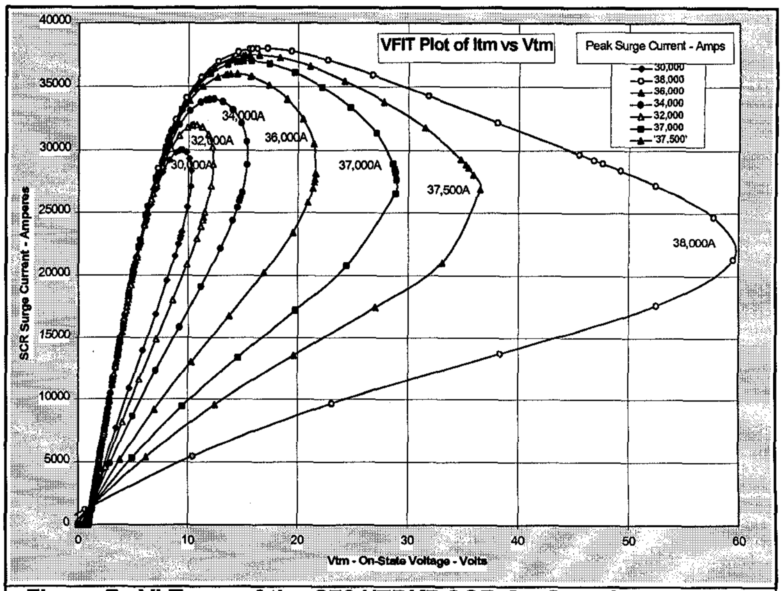

Figure 7. VI Trace of the C784/TBK7 SCR On-State Voltage Using the New PSPICE , VFIT Electro-thermal Model and Excel to Plot Results.

This is in agreement with theory as the temperature at which the thermally generated carriers approach the injected "intrinsic" carrier concentration in the device. The result is a rapidly decreasing spot resistivity, an increase in current density, and quick destruction of the device.

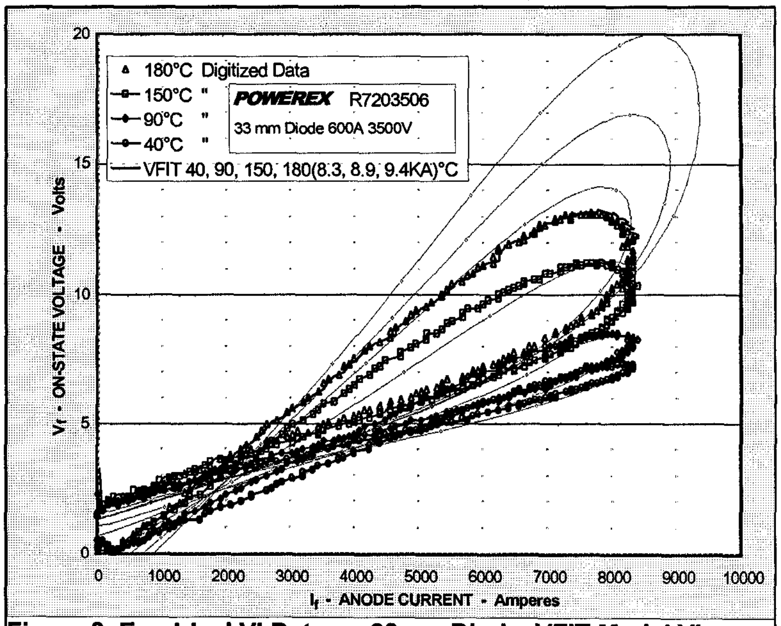

Figure 8. Empirical VI Data on 33mm Diode, VFIT Model VI Traces and VI Traces into area of Device Destruction

C. Waveforms of the Electro-thermal PSPICE™ SCR/Diode Model Simulating an Application

The waveforms of the electro-thermal PSPICE™ SCR/Diode models simulating an application requiring a 3 Cycle Surge Capability are Illustrated in Figure 9. The important thing to observe in this PSPICE™ Probe plot is that the peak surge current I(Rload) remains the same at about 25,000 Amps, while the peak on-state forward voltage drop V(A) continues to rise due to the higher junction temperature of each pulse. This increase in on-state forward voltage drop is reflected in higher peak power dissipation pulses and therefore, higher peak junction temperature V(Tj). The possibility of thermal runaway as observed in the parrot beak VI traces (see Figures 6 and 7) is apparent. The PSPICE™ net list, which created this graph is presented in the Appendix as Code Fragment No 2.

VI. CONCLUSIONS

Circuit modeling is an important tool in the design of power electronic applications. This paper has described a new mathematical model for SCRs and Diodes which includes the on-state forward voltage drop, the transient thermal impedance and the all important, virtual junction temperature. The model was demonstrated to be useful in SPICE type circuit simulators. The on-state model was extended to include the variation of the on-state voltage drop to the instantaneous junction temperature of the device. The resulting model should be capable of providing quick and accurate simulations of SCRs and Diodes in power electronic applications that can easily extend to multi-megawatt power levels.

The methodology to use these models in both non-electro-thermal and electro-thermal application requirements have been described including graphs of the output waveforms and quantitative evaluations of the overall accuracy. The agreement between the new mathematical models method and old, classical, but tedious, curve look up, superposition methods of calculating junction temperature was good. There was also shown to be good agreement between the empirical test values and the new Electro-Thermal PSPICE™ SCR(Diode) Model.

This SCR(Diode) modeling information hopefully will assist the power electronic engineer achieve more innovative, challenging and reliable designs in the many areas where power electronics can provide useful functions to the public.

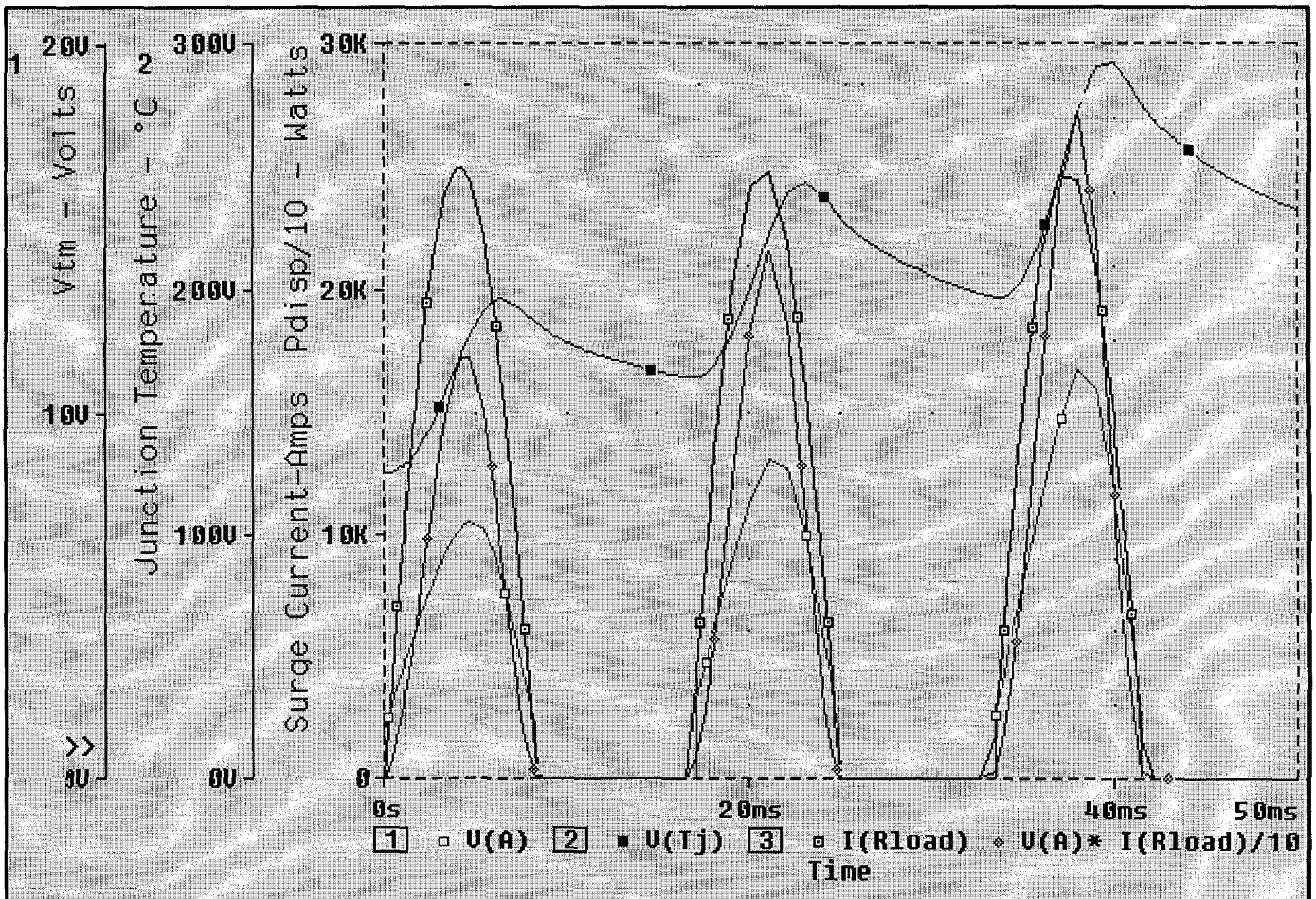

Figure 9. Waveforms of Application Using the New PSPICE SCR(Diode) Electro-Thermal Model

VII. REFERENCES

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VIII. APPENDIX: ISOTHERMAL and NON-ISOTHERMAL PSPICE™ NET LISTS for SCR(DIODE) RATING MODELS

Code Fragment 1. Net List for PSPICE SCR Modeling using Sub Circuit for SCR/Diode ABCD Model. Which Does NOT Account for the Increase in the On-State Voltage due to Junction Temperature

```
************** POWEREX TBK7 SCR  MODEL *************************************************************
* ANODE       A = ANODE input node
* CATHODE   K = CATHODE input node
* GATE        G = GATE input node
* Tj            Junction temperature output node
* AMB_T      Starting ambient temperature
****************************************************************************************************

.SUBCKT PRX_TBK7 A K G Kg Tj PARAMS:  AMB_T=27

*============================== Vtm MODEL ==============================
D_SCR     A   A1    Dmod  ;Provide SCR with Reverse Blocking [Designed for Vf = K = 0.4Volts]
EVtm      A1   K1    Value= {{A} + {B} * log(Abs(I(V_Pwr_Sen))) + {C} * I(V_Pwr_Sen) +
                                                        {D} * PWR(I(V_Pwr_Sen),.5)-0.4}
**EVtm     A1   K1  Value= {{M} + {N} *PWR(I(V_Pwr_Sen),.25)  + {O} *PWR(I(V_Pwr_Sen),.5) +
**                                      {P} *PWR(I(V_Pwr_Sen),.75) + {Q} * I(V_Pwr_Sen)-0.4}
Sscr       K1    k2  G2    Kg    SMOD  ;Voltage Controlled Switch
Rg           G     Kg      1              ;Gate Resistor
V_Pwr_Sen  K2  K

*========================== THERMAL MODEL ==========================
G_PowerM  0      Tj    Value= {I(V_Pwr_Sen) * (V(A1,K1)+0.4)} ; <=====I(power) for ThZ Model
R1      Tj     Tj1    {R1}
C1      Tj     Tj1  {TAU1/R1}
R2      Tj1    Tj2    {R2}
C2      Tj1    Tj2  {TAU2/R2}
R3      Tj2    Tj3    {R3}
C3      Tj2    Tj3  {TAU3/R3}
R4      Tj3    Tj4    {R4}
C4      Tj3    Tj4  {TAU4/R4}
R5      Tj4     0     {R5}
C5      Tj4     0   {TAU5/R5}
* * * *  Other Models * * * *
.Model Dmod D(Eg = 0.9 Cjo = 1.0uf) ; ["Ideal" except for: Vf = K = 0.4Volts]
.Model SMOD VSWITCH(RON=1E-7  ROFF=1E+5  VON=1  VOFF=0)
.ENDS ;************************END OF SCR SUBCIRCUIT MODEL*********************************
```

Code Fragment 2. Net List for PSPICE SCR Modeling using Sub Circuit for SCR/Diode Model. Which DOES Account for the Increase in the On-State Voltage due to Junction Temperature

```
**** 11/19/97 ******** PSpice  Ver 7.1 (October 1996) POWEREX  TBK7  MODEL 77mm ***************************
.OPT ACCT NOMOD NOPAGE RELTOL=.001 ABSTOL=1uA ITL5=0  EXPAND
.tran  1us  50ms 1ns ;<=====I(power) for Sine Wave Current  Vtm & Tj
**************    TBK7 Transient Thermal Response Parameters ****************************************************
.param R1 =  6.59832688785955E-05,        TAU1 = 2.727159E-04
.param R2 =  1.00802536313663E-04,        TAU2 = 2.478587E-03
.param R3 =  8.62792998426455E-04,        TAU3 = 1.502316E-02
.param R4 =  4.49074599479524E-03,        TAU4 = 0.1969325
.param R5 =  6.47953113196889E-03,        TAU5 = 1.241345
**** VFIT Formula Parameters*****************************************************************************
.param PS =  {((0.00019-0.000113)/(160.-25.))} ; =(mh-mc)/(Tsc-Tsh)     = Del Vfit Slope / Del Ts
.param PE= {(0.09/191.)}   ;Del n / Del Tj = Del n / (peak Tjc)/ (peak Tjh) = Del n  for increas in witdh of loops
* .pram NX={(log((Vh1-Vc)/(Th1-Tc)) - log((Vh2-Vc)/(Th2-Tc)))/((log((Th1-Tc)/2) - log((Th2-Tc)/2)) ;  Eq 6.
******************** INCLUDE THE MODEL ********************************************************************
*******.INC TBK7.CIR  ; Not Used at this time

******************* POWEREX TBK7 SCR  MODEL *****************************************************************
* ANODE    A= ANODE input node        CATHODE  K=CATHODE input node      GATE   G=Gate input node
* Tj         Junction temperature output node     AMB_T    Starting ambient temperature
**************************************************************************************************************
.SUBCKT PRX_TBK7 A  K  Tj  PARAMS:  T_Amb=27
************ Vtm VFIT Model *********  November 19, 1997 ****************************************************
D_SCR A   A1    Dmod  ; Provide SCR with Reverse Blocking
***********EVtm  A1  K1 Value={1.25+(0.000113 + {PS}*(160+(V(Tj,0))^(1.2+{PE}*(V(Tj,0)-117))-25))*(I(V_Pwr_Sen)-1500)}
EVtm  A1  K1 Value={1.25+(0.000113 + {PS}*({T_Amb}+(V(Tj,0)-{T_Amb})^(1.2+{PE}*(V(Tj,0)-117.-{T_Amb})) -
                                   25.))*(I(V_Pwr_Sen)-1500.)}
Sscr      K1    K2   G2     KG     SMOD  ;Voltage Controlled Switch
Rg        G      KG       1                    ; Gate Resistor
V_Pwr_Sen  K2  K                              ; Current Shunt
******** Analog Thermal Model **** {1A = 1W dissipated in device}  {1V = 1øC Junction Temp Rise)  **************
G_PowerM   0      Tj  Value= {ABS(I(V_Pwr_Sen)*(V(A1,K1)+0.4))} ;;;+83.33*{AMB_T}} ; <=====I(power) for ThZ Model
R1         Tj      Tj1     {R1}
C1         Tj      Tj1  {TAU1/R1}
R2         Tj1    Tj2     {R2}
C2         Tj1    Tj2  {TAU2/R2}
R3         Tj2    Tj3     {R3}
C3         Tj2    Tj3  {TAU3/R3}
R4         Tj3    Tj4     {R4}
C4         Tj3    Tj4  {TAU4/R4}
R5         Tj4    Tamb      {R5}
C5         Tj4    Tamb  {TAU5/R5}
VAMB       Tamb     0   {T_Amb} ;Tambient Temp Value
* * * *Other  Models * * * *
.Model Dmod D(Eg = 0.9 Cjo = 1.0uf) ; ["Ideal" except for: Vf = K = 0.4Volts]
.Model SMOD VSWITCH(RON=1E-7  ROFF=1E+5  VON=1  VOFF=0)
.ENDS          ;----- END OF SCR SUBCIRCUIT MODEL

****************************** TEST CIRCUIT  ***************************************************************
V_SourceGen  Vsource   0    sin(0 25000 60) ;  <==Itm for Vtm see Next   31kA Itsm 1 Cy  60 Hz
Rload      Vsource   A     1      ;One Ohm Load Resistor
* * SET UP THE SCR SUBCIRCUIT * *
XSA  A  0  Tj  PRX_TBK7    PARAMS:T_Amb=125
.probe
.END
```