Abstract – The 5th generation IGBT device, Carrier Stored Trench Bipolar Transistor (CSTBT), has been recently introduced in the market. This newer generation IGBT represents the current state of the art with its excellent electrical characteristics. In this work, the physics-based electro-thermal Leturcq-Palmer IGBT model, which has been proven robust by the validation with NPT and PT IGBTs, is used to simulate the behavior of the CSTBT. The hard switching experiments have been performed using inductive and resistive loads under different temperature conditions. The simulation results from the model are compared with the experimental results under different conditions to validate the model accuracy.

I. INTRODUCTION

The 5th generation IGBT device, Carrier Stored Trench Bipolar Transistor (CSTBT), has been recently introduced in the market. Combining light punch through (LPT) technology and optimized fabrication processing, this newer generation IGBT has state-of-the-art characteristics, such as low saturation voltage, low turn-off switching loss, rugged SOA [1-2]. Compared with the 4th generation IGBT, the conventional trench-gate punch-through IGBT, the new device has a reduced gate charge, and consequently requires lower driving power. With its above superior characteristics, CSTBT will definitely further improve the IGBT performance in its wide application field, especially the high frequency industrial power supply field. Therefore, it is necessary to model this promising new generation device, while only some characterization and no modeling work have been presented in the literature to date.

A complete physics-based IGBT circuit simulator model has been presented before [3-4]. Its high accuracy has been validated by various structure IGBTs. Its usefulness is enhanced by its practical parameterization procedure and reasonable simulation speed [5]. In this work, the analytical electro-thermal IGBT model, suitable for other previous structure IGBTs, has been modified to simulate the behavior of the CSTBT. The hard switching experiments have been performed using inductive and resistive loads under different temperature conditions. Comparison between the experimental and simulated results is performed to validate the high degree of accuracy of the model developed.

II. THE 5TH GENERATION IGBT- CSTBT

A. Stored Carrier Concept

The application of trench gate technology in the 4th generation IGBT significantly reduced the IGBT saturation voltage drop because it greatly reduces wide-drift-region voltage drop, the dominating component of the total IGBT saturation voltage. The key reason for this reduction is that the trench IGBT enhances the conductivity modulation in the drift region (PIN effect) with a carrier distribution similar to that of the pin diode, instead of the tending-to-zero carrier concentration near the emitter side, happening in the planar gate IGBT. Therefore, trench IGBT realizes the original concept of IGBT, “IGBT = pin diode + MOSFET”.

To further improve the carrier concentration at the emitter side, Carrier Stored Trench Bipolar Transistor (CSTBT) is fabricated with an additional n type buried layer at the emitter side, as shown in the cell structure diagram of the CSTBT in Fig. 1(a). Compared with the conventional high cell density trench IGBT structure shown in Fig. 1 (b), the introduction of an additional buried layer provides “stored” carriers to increase carrier concentration near the emitter side of the device. With the unique structure similar to that of the ideal pin diode, the carrier distribution in the n+ drift region of CSTBT becomes closer to that of a pin diode, resulting in an increased conductivity in the n+ layer. The final result is a substantial reduction in the on-state voltage of the device. Fig. 2 shows the n+ drift region carrier distribution comparison of diode, conventional trench IGBT and CSTBT.

![Fig. 1. IGBT cell structure comparison: (a) CSTBT, (b) Conventional PT trench IGBT](image-url)
Fig. 2. Qualitative comparison of carrier distribution in a PIN diode, a conventional trench IGBT and in the CSTBT.

B. Light Punch Through Concept

In addition to the stored carrier concept, optimized vertical structure based Light Punch-Through (LPT) technology is also applied in the CSTBT. With the selected thickness of the n- drift region, the depletion region extends to the collector in the off-state but does not reach the buffer layer at normal operating voltages. Thus the key of LPT technology, similar to Field Stop concept proposed by the European manufacturers, is to use the n+ buffer layer to support voltage as rated voltage is approached, but support the field entirely in the drift region when normal operating voltages are applied. Consequently, the n- drift region will be optimized to be thin enough to provide low V_CESAT while maintaining a robust switching SOA. An added advantage of the LPT structure is efficient switching characteristics with no need for carrier lifetime control processing due to the controlled carrier concentration in the n- region during conduction as a result of the optimized n+ buffer and p+ collector layers.

III. PHYSICS-BASED IGBT CIRCUIT SIMULATOR MODEL

A. Fourier-based-solution Approach

Among many analytical IGBT modeling approaches presented in the literature, Fourier-based-solution (FBS) approach has a better trade-off between the accuracy and simulation speed, and has been firmly established after extensive experimental validation and parameterization. The key of this approach is the physics-based description of the carrier distribution in the IGBT n drift region.

Like other conductivity-modulated devices, the behavior of an IGBT depends heavily on the carrier distribution in the wide base region, and the ambipolar carrier diffusion equation (ADE) describes the carrier dynamics in this region under high-level injection conditions.

\[ D \frac{\partial^2 p(x,t)}{\partial x^2} = \frac{\partial p(x,t)}{\partial t} + \frac{\partial p(x,t)}{\partial t} \]

where \( D \) is the ambipolar diffusion coefficient, \( \tau \) is the high-level carrier lifetime within the drift region and \( p(x,t) \) is the excess carrier concentration. Therefore, solving the ADE is the key to modeling the IGBT behavior.

After applying the Fourier transformation to the ADE, the drift region carrier distribution can be represented with the equivalent RC network shown in Fig. 3. The detailed discussion of the FBS approach and the corresponding equivalent circuit implementation can be found in [5] and [6].

The representation requires the width of the undepleted base region and the hole and electron currents at the boundaries of the region \( (x_1 \text{ and } x_2) \), from which one can calculate the gradients of the carrier concentrations, \( f(t) \) and \( g(t) \) at \( x_1 \) and \( x_2 \), respectively. The functions \( f(t) \) and \( g(t) \) are defined as follows:

\[ f(t) = \left[ \frac{\partial p(x,t)}{\partial t} \right]_{x_1} = \frac{1}{2qA} \left[ \frac{I_{n1}}{D_n} - \frac{I_{p1}}{D_p} \right] \]

\[ g(t) = \left[ \frac{\partial p(x,t)}{\partial t} \right]_{x_2} = \frac{1}{2qA} \left[ \frac{I_{n2}}{D_n} - \frac{I_{p2}}{D_p} \right] \]

A is the cross-sectional area of the device, \( D_n \) and \( D_p \) the electron and hole diffusion coefficients, \( I_{n1} \) and \( I_{p1} \) the electron and hole currents at \( x = x_1 \) (p+ side), and \( I_{n2} \) and \( I_{p2} \) the electron and hole currents at \( x = x_2 \) (p-body side). The variable definition is shown in Fig. 4. Clearly, the success of the approach now depends solely upon developing the appropriate boundary conditions — hole and electron currents at the edges of the drift region.

The different IGBT structures have different boundary current definitions. For example, the electron current at emitter side \( (I_{n1}) \) of NPT IGBT is given in Equation (4):

\[ I_{n1} = \int_{x=0}^{x=0} \left[ \frac{\partial p(x,t)}{\partial t} \right] \]

Fig. 3. Equivalent circuit to describe drift region carrier distribution

Fig. 4. Boundary condition definition for the PT IGBT
where \( P \) is the recombination parameter, while the hole current at emitter side \( I_{p1} \) of PT IGBT is obtained by Equation (5):

\[
I_{p1} = \frac{qAD_{pH}H}{L_{PH}pH} \left[ P_{H0} - P_{HW} \frac{W_H}{L_{PH}} \right] + I_{QH}
\]

where \( D_{pH} \) is hole diffusion coefficient in the buffer layer, \( L_{PH} \) is excess carrier diffusion length and the term \( I_{QH} \) represents the capacitive current due to variations in the charge \( Q_H \) stored in the buffer layer.

Once one current component is defined, the other current component can be obtained from the current continuity equation:

\[
I_A = I_{a1} + I_{p1} = I_{a2} + I_{p2}
\]

IV. PARAMETER EXTRACTION

Another advantage of FBS approach is its practical parameter extraction described in [5]. Since CSTBT is based on the PT structure, the parameter extraction procedure, proposed before for the PT IGBT, is also suitable for the CSTBT, with some modification.

The CSTBT model has thirteen parameters as the PT IGBT. Most parameters can be obtained based on the manufacturer’s datasheet or simple static measurements, especially for gate and geometry parameters. The only experiment needed is the turn off testing with the inductive load under variable collector-emitter voltage conditions to extract two dominant parameters in the model: high-level lifetime in the n drift region and the low-level lifetime in the high-doped n⁺ buffer. Only datasheet data and the inductive turn off experiment data were used for the parameter extraction. No additional information from the manufacturer was used.

The short channel parameter (\( \lambda \)) can be obtained directly from the known I-V characteristic curve shown in Fig.5. MOS threshold voltage \( V_{th} \) and Transconductance Coefficient \( K_{pl} \) can be obtained indirectly from the equations:

\[
i_c = K_{ppl} (V_{GS} - V_{th})^2
\]

\[
K_{ppl} = 2K_{ppl}
\]

Gate-emitter capacitance \( C_{ge} \) can be directly obtained from the input capacitance \( C_{i} \) (measured gate-emitter capacitance when collector is shorted to emitter) provided in the datasheet and it can be chosen equal to \( C_{i} \) at 10V. MOS oxide capacitance \( C_{ox} \) is the maximum value of the Miller capacitance when the depletion region under the gate area has not formed \( (C_{dep} = 0) \), i.e.

\[
C_{ox} = Max(C_{rev})
\]

The active die area \( A \) can be estimated empirically as:

\[
A \approx \frac{I_{CM}}{J}
\]

where \( I_{CM} \) is the peak collector current rating from the RBSOA curve given in the datasheet and the current density \( J \) ranges typically from 100 A/cm² to 150 A/cm². The intercell ratio can be chosen as:

\[
a = \frac{C_{rev}}{C_{rev}}
\]

For the doping concentration \( N_B \) and the n⁺ drift region width, the extraction procedure is modified from the description of [5] to account for the light punch through structure. The breakdown voltage \( V_{BR} \) of a NPT device is given by

\[
V_{BR}(w_B) = \frac{qN_B}{2\varepsilon}w_B^2
\]

and the breakdown voltage for a punch through device is

\[
V_{BR}(w_B) = E_c.w_B - \frac{1}{2} \frac{qN_B}{\varepsilon}w_B^2
\]

where \( E_c \) is the critical electrical field value for silicon. These two equations can be plotted as a function of drift region width \( w_B \) as shown in Fig. 6 for \( N_B = 1\times10^{19} \) cm⁻³. As can be seen from the figure, this doping concentration gives a maximum breakdown voltage of approximately 1330V. The intersection of the two curves represents the drift region width at which avalanche and punch through occur for the same voltage. A punch through design would typically have a drift region width within the PT region identified in the figure, and a non punch through design would be within the NPT region. The breakdown voltage advantage of PT for the same drift region width can be clearly seen in the figure. The light punch through region is located between the PT and NPT region. From these considerations, the drift region width for the 1200V CSTBT under consideration is estimated to be 120µm.

The lifetime extraction of the CSTBT is based on the experimental data acquired in the clamped inductive load circuit. As shown in Fig. 7 for a PT IGBT, the high-level carrier lifetime \( \tau_{HL} \) corresponds to the low-voltage...
\( \tau_{\text{eff}} \) value, while the low-level carrier lifetime in the buffer layer \( \tau_{\text{BF}} \) is equal to the \( \tau_{\text{eff}} \) value at high clamped voltage since the drift region is depleted under that condition.

![Graph showing breakdown voltage as a function of drift region width](image)

Fig. 6. Breakdown voltage as a function of drift region width (in cm) for the NPT and PT case for \( \text{NB} = 1 \times 10^{14} \text{cm}^{-3} \). The NPT, LPT and PT regions are identified in the figure.

Upon the consideration of simplicity and negligible loss of accuracy, the remaining parameters of the buffer layers can be obtained based on their empirical value range. The typical PT IGBT buffer layer width \( W_B \) is about 4–10 \( \mu \text{m} \). The normal range of the doping concentration \( N_H \) is \( 10^{16} \text{–} 10^{17} \text{cm}^{-3} \). Smaller \( W_B \) and \( N_H \) values should be chosen for the CSTBT.

Summarized in the table below are the extracted parameters of CSTBT.

<table>
<thead>
<tr>
<th>Part</th>
<th>Symbol</th>
<th>Description</th>
<th>Extracted Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS Gate</td>
<td>( V_{TH} )</td>
<td>MOS threshold voltage</td>
<td>8.2</td>
</tr>
<tr>
<td></td>
<td>( R_{GP} )</td>
<td>MOS transconductance coefficient</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>( \lambda )</td>
<td>Short-channel parameter</td>
<td>0.03</td>
</tr>
<tr>
<td></td>
<td>( C_{BE} )</td>
<td>Gate-emitter Capacitance</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td>( C_{ox} )</td>
<td>Oxide Capacitance</td>
<td>8</td>
</tr>
<tr>
<td>Geom.</td>
<td>( A ) (( \text{cm}^2 ))</td>
<td>Effective Die Area</td>
<td>1.3</td>
</tr>
<tr>
<td></td>
<td>( \alpha_i )</td>
<td>Ratio of intercell to total die area</td>
<td>0.2</td>
</tr>
<tr>
<td>BJT Body</td>
<td>( W_B ) (( \text{um} ))</td>
<td>N drift region Width</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td>( N_B ) (( \text{cm}^{-3} ))</td>
<td>Doping concentration of N drift region</td>
<td>( 1 \times 10^{14} )</td>
</tr>
<tr>
<td></td>
<td>( \tau_{\text{hi}} ) (( \text{um} ))</td>
<td>Carrier high-level lifetime in N drift</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>( N_H ) (( \text{cm}^{-3} ))</td>
<td>Doping concentration of N buffer layer (PT)</td>
<td>( 0.8 \times 10^{16} )</td>
</tr>
<tr>
<td></td>
<td>( W_H ) (( \text{um} ))</td>
<td>Width of a(^{+}) buffer layer (PT)</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>( \tau_{\text{BF}} ) (( \text{um} ))</td>
<td>Carrier lifetime in N buffer layer (PT)</td>
<td>0.015</td>
</tr>
</tbody>
</table>

V. Experimental and Simulated Results

For the purpose of model validation, some characterization experiments have been performed. Fig. 8 shows the positive temperature coefficient of the saturation voltage drop, which is different from the slightly negative temperature coefficient of the 4\(^{th}\) generation IGBT (Trench PT). Fig. 9 shows CSTBT chip turn-off current family at resistive and inductive load condition under different temperatures. Within the whole operational temperature range, the current falling times are about 1 \( \mu \text{s} \) under both circuit conditions.

![Graph showing CSTBT saturation voltage drop variation under different temperatures](image)

Fig. 8. CSTBT \( V_{ce(on)} \) variation with temperature
The comparison between the experiment and simulation results under inductive load at 27 °C and 125 °C are shown in Fig. 10(a) and (b), respectively. The collector-emitter voltage is 600 V, the current is 100A and the horizontal scale is 200ns/div. The good match shown in the figures strongly demonstrates the accuracy of the model.

VI. DISCUSSION AND CONCLUSIONS

The 5th generation IGBT device, CSTBT, is presented firstly with its superior characteristics such as low saturation voltage, low turn-off switching loss and rugged SOA. Then the Fourier-based-solution physics-based IGBT modeling approach is briefly reviewed. Then the IGBT parameter extraction described in [5] is applied to the CSTBT to determine the model parameters. By jointly using three general parameter extraction methods – empirical-value-based extraction, datasheet-based extrapolation, and simple-test-based extraction – the total extraction procedure only needs a simple clamped inductive load test for the extraction of the thirteen parameters needed for the LPT CSTBT model. Simulation results for the inductive turn off are compared with experimental results at two different temperatures and excellent agreement is obtained.

The model actually used in the simulation does not contain a description of the buried layer. In future work, we will add to the model a description of the buried layer following the same approach described in [4] to model the buffer layer in a PT or FS IGBT.

In conclusion, the satisfactory matching between the simulation results and actual experimental results strongly proves the accuracy of the electro-thermo, physics-based LPT CSTBT model and further demonstrates the practicality of the parameter extraction method presented.

ACKNOWLEDGMENTS

This work was supported by the U.S. Office of Naval Research under Grant No. N00014-00-1-0131.
REFERENCES


