Trench-Gate Technology for The Next Generation of MOS Power Devices

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Introduction

1. The Trench Gate
   Structure, Development History and Advantages

2. Low Voltage MOSFETs
   $R_{DS(on)}$, Small packages, $Q_G$, Future Direction

3. High Power IGBT Modules for Industrial Applications
   Low $V_{CE(sat)}$, Low losses, Reduced EMI/RFI

4. Special Devices
   Strobe Flash, Fork Lift, Microwave Oven

5. Conclusion
Planar versus Trench-Gate MOSFET Unit Cell Comparison

**Planar Gate Cell**

- Source
- Gate
- Drain
- \( R_{\text{Channel}} \)
- \( R_{n-} \)
- \( R_{\text{JFET}} \)

**Trench Gate Cell**

- Source
- Gate
- Drain
- \( R_{\text{Channel}} \)
- \( R_{n-} \)
Advantages of Trench-Gate:

- Vertical channel requires less area compared to the horizontal channel of planar structure
  - Greater cell density
  - Greater channel width/unit area
  - Lower $R_{DS(on)}$

- No $R_{JFET}$ between adjacent cells
  - Greater cell density
  - Lower $R_{DS(on)}$
Major Mitsubishi/Powerex Trench-Gate Milestones:

1983 - Trench capacitor cell proposed for next generation DRAM
1988 - Mass production of trench capacitor memory launched
1992 - Prototype low voltage trench gate MOSFETs developed
1994 - Mass production of trench gate 30V-150V MOSFETs launched
1994 - Prototype 600V Trench IGBT developed
1994 - 400V Strobe Flash IGBT production started
1995 - 250V 400A, 600A Trench gate IGBT module production started
1998 - 1200V Trench IGBT developed
1999 - Production of 600V, 1200V trench gate IGBT modules started
1999 - Production of sub μm trench MOSFETs started
Trench-Gate MOSFET Technology Focus:

- Low voltage types 20V - 150V
- N-channel and P-channel
- Logic level drive 4V and 2.5V
- Low $R_{DS(ON)}$ in small packages
- Low $Q_G$
- Low $R_{DS(ON)}$ at low driving voltage
- Preserve ESD ruggedness
Low voltage MOSFETs benefit most from trench gate:

<table>
<thead>
<tr>
<th>% of $R_{DS(ON)}$</th>
<th>Typical 60V High Density Planar Gate MOSFET</th>
<th>Typical 500V MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{CH}$</td>
<td>30%</td>
<td>10%</td>
</tr>
<tr>
<td>$R_{JFET}$</td>
<td>20%</td>
<td>5%</td>
</tr>
<tr>
<td>$R_{N-}$</td>
<td>30%</td>
<td>80%</td>
</tr>
<tr>
<td>Other</td>
<td>20%</td>
<td>5%</td>
</tr>
</tbody>
</table>

Trench technology attacks $R_{CH}$ and $R_{JFET}$
Trench-Gate MOSFET Chip Structure:

- Source Electrode
- Source Layer
- Polysilicon Gate
- Gate Oxide
- P-base
- n-epi layer
- n+ Drain Electrode

5th Generation stripe trench 1μm design rule
Benchmark TO220 (D²-Pak) Devices:

\( R_{\text{DS(ON)}} \) (mΩ) Maximum, \( V_{\text{GS}}=10V, T_j=25\text{C} \)

<table>
<thead>
<tr>
<th>( V_{\text{DSS}} ) n-ch, -( V_{\text{DSS}} ) p-ch (Volts)</th>
<th>20V</th>
<th>30V</th>
<th>60V</th>
<th>100V</th>
<th>150V</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-ch</td>
<td>4.0</td>
<td>4.7</td>
<td>12</td>
<td>7.0</td>
<td>19</td>
</tr>
<tr>
<td>p-ch</td>
<td>4.0</td>
<td>4.7</td>
<td>12</td>
<td>7.0</td>
<td>19</td>
</tr>
</tbody>
</table>

More than 500 types available in TO-220, TO-220 Isolated, D²-Pac, D-pac. Standard and logic level (4V, 2.5V) drive. n-channel and p-channel

New - FS100VSJ-02A
Reducing $Q_g$: For DC to DC converter and synchronous rectification applications:

<table>
<thead>
<tr>
<th>Package</th>
<th>Type</th>
<th>Process</th>
<th>$V_{DSS}$</th>
<th>Max $R_{DS(on)}$</th>
<th>$C_{iss}$</th>
<th>$Q_g$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOP-8</td>
<td>FY10AAJ-03</td>
<td>Conventional Trench</td>
<td>30V</td>
<td>13.5mΩ</td>
<td>2850pF</td>
<td>32nC</td>
</tr>
<tr>
<td>SOP-8</td>
<td>FY10AAJ-03A</td>
<td>Shallow Trench</td>
<td>30V</td>
<td>13.5mΩ</td>
<td>1800pF</td>
<td>22nC</td>
</tr>
</tbody>
</table>

**DC to DC Converter Efficiency**

$V_{IN}=15V$, $V_{OUT}=3.3V$, $f=300kHz$

- **FY10AAJ-03A**: 30% Reduction of Gate Charge
Low $R_{DS(ON)}$ in small package:

<table>
<thead>
<tr>
<th>Package</th>
<th>Type</th>
<th>Process</th>
<th>$V_{DSS}$</th>
<th>Max $R_{DS(on)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOP-8</td>
<td>FY7ACH-03A Dual n-channel</td>
<td>5\textsuperscript{th} Generation Shallow Trench</td>
<td>30V</td>
<td>26m\Omega</td>
</tr>
<tr>
<td>TSSOP-8</td>
<td>FY7BCH-02A Dual n-channel</td>
<td>5\textsuperscript{th} Generation Mesh Trench</td>
<td>20V</td>
<td>25m\Omega</td>
</tr>
</tbody>
</table>
Low $R_{DS(ON)}$ at low drive voltage:

<table>
<thead>
<tr>
<th>Package</th>
<th>Configuration</th>
<th>Type Number</th>
<th>Max $R_{DS(ON)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOP-8</td>
<td>Single n-channel</td>
<td>FY10AAJ -03A</td>
<td>20m$\Omega$</td>
</tr>
<tr>
<td>SOP-8</td>
<td>Single p-channel</td>
<td>FY8ABJ -03</td>
<td>37m$\Omega$</td>
</tr>
<tr>
<td>SOP-8</td>
<td>Dual n-channel</td>
<td>FY8ACH-02A</td>
<td>36m$\Omega$</td>
</tr>
<tr>
<td>TSSOP-8</td>
<td>Dual n-channel</td>
<td>FY7BCH-02A</td>
<td>37m$\Omega$</td>
</tr>
</tbody>
</table>

Don’t be fooled - Industry standard is to supply maximum $R_{DS(ON)}$ at $V_{GS}=10V$ for logic level (4V drive) devices and $V_{GS}=4V$ for 2.5V drive devices.

**Powerex/Mistubishi provides maximum $R_{DS(ON)}$ specified at low drive voltage for all logic level (4V, 2.5V) devices**
Preserving ESD ruggedness:

Two methods to reduce $R_{DS(ON)}$ at low drive voltages

1. **Increase channel width/unit chip area** - Trench gate structure is very effective for this approach.

2. **Reduce gate oxide thickness** - This approach degrades $V_{GSS}$ and ESD ruggedness.

![Diagram](image)

ESD Withstanding (Human Body Model)

- **Test Voltage**
  - 4000V
  - 3000V
  - 2000V
  - 1000V

- **Samples**
  - 10
  - 20
  - 30
  - 40

- **Test Results**
  - FY10AAJ-03A (No failures)
  - Competitive Device
More ESD ruggedness:

Adopt an integrated gate protection zener

<table>
<thead>
<tr>
<th>Package</th>
<th>Type</th>
<th>Process</th>
<th>$V_{DSS}$</th>
<th>Max $R_{DS(on)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSSOP-8</td>
<td>FY6BCH-02E Dual n-channel</td>
<td>5th Generation Mesh Trench</td>
<td>20V</td>
<td>30mΩ</td>
</tr>
<tr>
<td></td>
<td>With integrated G-S zener</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSSOP-8</td>
<td>FY7BCH-02E Dual n-channel</td>
<td>5th Generation Mesh Trench</td>
<td>20V</td>
<td>27mΩ</td>
</tr>
<tr>
<td></td>
<td>With integrated G-S zener</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Trench-gate MOSFET future direction:

Next Step - Sub $\mu$m design trench

<table>
<thead>
<tr>
<th>Package</th>
<th>Type</th>
<th>Process</th>
<th>$V_{DSS}$</th>
<th>Max $R_{DS(on)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSSOP-8</td>
<td>FY7BCH-02B</td>
<td>Proprietary</td>
<td>20V</td>
<td>21mΩ</td>
</tr>
<tr>
<td></td>
<td>Dual n-channel</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSSOP-8</td>
<td>FY8BCH-02</td>
<td>Proprietary</td>
<td>20V</td>
<td>19mΩ</td>
</tr>
<tr>
<td></td>
<td>Dual n-channel</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

More types under development....
Trench-Gate IGBT Modules
(For High Power Industrial Applications)

Technology Focus:
• Low $V_{CE(sat)}$, Low Losses
• Full Line-Up 600V and 1200V
  50A-600A
• High Reliability
• Reduced EMI/RFI
Advantages of Trench-Gate Structure for IGBT:

- Vertical channel requires less area compared to the horizontal channel of planar structure
  - Greater cell density
  - More uniform current flow through chip
  - Robust Turn-Off Switching Capability

- No $R_{JFET}$ between adjacent cells
  - Greater cell density
  - Lower $V_{CE(SAT)}$
Reducing $V_{CE(sat)}$:

<table>
<thead>
<tr>
<th>Components of $V_{CE(sat)}$</th>
<th>Reduction Technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{Channel}$</td>
<td>Adopt trench gate surface structure to increase cell density and channel width per unit area</td>
</tr>
<tr>
<td>$R_{JFET}$</td>
<td>Eliminate by adopting trench gate structure</td>
</tr>
<tr>
<td>$R_{n-}$</td>
<td>Utilize optimized PT chip design with local lifetime control to increase on-state carrier concentration</td>
</tr>
</tbody>
</table>
IGBT Structure Comparison:

PT IGBT
- Poly-Si Gate
- n⁻ drift region
- n⁺ buffer layer
- p⁺ anode
- Collector Electrode

NPT IGBT
- Poly-Si Gate
- n⁻ drift region
- Emitter Electrode
Advantages of PT structure:

- $n^-$ layer thickness and resistivity can be optimized for low $V_{CE\text{(sat)}}$ without special thin wafer processing or leakage current stability problems.

- Low $V_{CE\text{(sat)}}$ at elevated junction temperature

- Tail current time is short (due to lifetime control) (~$0.3\mu$s versus several $\mu$s for NPT)

- Low leakage current at high temperatures (one tenth to one twentieth of thin $n^-$ NPT)
Effect of Local Lifetime Control Using Heavy Ion Irradiation:

• Carrier lifetime in the n+ buffer layer is reduced using local life time control
• Long lifetime is maintained in the n- layer
• Carrier concentration in the n- layer during conduction is increased
• Rn- is reduced

$V_{CE(sat)}$ is Reduced
Maintaining Short Circuit Withstanding:

Adopt RTC (Real Time Control Circuit) to clamp short circuit current
1200V Trench Gate IGBT Performance:

$E_{SW\text{(off)}}$ versus $V_{CE\text{(sat)}}$ Trade-Off

$V_{CE\text{(sat)}}$ (V)

$T_j=125^\circ C$

$I_C=100A$

$E_{SW\text{(off)}}$ (mJ/pulse) $T_j=125^\circ C$, $I_C=100A$, $V_{CC}=600V$
Characteristics of 1200V (F-Series) trench gate IGBT:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>3\textsuperscript{rd} Gen. Planar</th>
<th>Trench</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CE(sat)}$</td>
<td>$T_j=125\degree C$</td>
<td>2.85V</td>
<td>1.9V</td>
</tr>
<tr>
<td>SWSOA</td>
<td>$2X I_{C(rated)}$</td>
<td>Square</td>
<td>Square</td>
</tr>
<tr>
<td>$t_{SC}$</td>
<td>Short Circuit Withstand Time</td>
<td>$&gt;10\mu s$</td>
<td>$&gt;10\mu s$</td>
</tr>
<tr>
<td>$E_{SW(off)}$</td>
<td>Turn-Off Switching Energy (Normalized)</td>
<td>1.0</td>
<td>0.8</td>
</tr>
</tbody>
</table>
## Characteristics of 600V (F-Series) trench gate IGBT:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>3rd Gen. Planar</th>
<th>Trench</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CE\text{(sat)}}$</td>
<td>$T_j=125$C</td>
<td>2.6V</td>
<td>1.6V</td>
</tr>
<tr>
<td>SWSOA</td>
<td>$2X I_{C(rated)}$</td>
<td>Square</td>
<td>Square</td>
</tr>
<tr>
<td></td>
<td>Current Density</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SC}$</td>
<td>Short Circuit</td>
<td>$&gt;10\mu s$</td>
<td>$&gt;10\mu s$</td>
</tr>
<tr>
<td></td>
<td>Withstand Time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$E_{SW\text{(off)}}$</td>
<td>Turn-Off Switching Energy (Normalized)</td>
<td>1.0</td>
<td>0.75</td>
</tr>
</tbody>
</table>
Next Generation Performance:

1200V F-Series IGBT Module

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Third Generation H-Series</th>
<th>Trench Gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CE(sat)} ~ (V) ~ T_j=125C$</td>
<td>2.3</td>
<td>1.9</td>
</tr>
<tr>
<td>Switching Loss - $E_{on}+E_{OFF}$</td>
<td>1.0</td>
<td>0.85</td>
</tr>
<tr>
<td>Total Sinusoidal Output Inverter Loss $f_{PWM}=10KHz$</td>
<td>1.0</td>
<td><strong>0.70</strong></td>
</tr>
<tr>
<td>Thermal Impedance $R_{TH(i-c)}$</td>
<td>1.0</td>
<td>1.45</td>
</tr>
<tr>
<td>Temperature Rise - $T_{J-C}$</td>
<td><strong>1.0</strong></td>
<td><strong>1.0</strong></td>
</tr>
</tbody>
</table>

30% Reduction of losses!
Evolution of Industrial Power Semiconductor Modules:

**Chip Technology**
- Darlington Transistor
- High-β
  - G1 IGBT
  - G2 IGBT

**Package Technology**
- Conventional Al$_2$O$_3$
- Al$_2$O$_3$ DBC
- AlN DBC (Soldered Power Terminals)
- Generation 3 IGBT
- Trench
- U-Package
New Module Package

Conventional Module (H-Series)
- Main Terminal Electrode
- Silicone Gel
- Epoxy Resin
- Molded Case
- Solder Connection
- Cu Base Plate
- Power Chips
- AlN Substrate

New Module (U-Package)
- Main Terminal Electrode
- Silicone Gel
- Cover
- Insert Molded Case
- Al Bond Wires
- Cu Base Plate
- Power Chips
- AlN Substrate
Advantages of the New Module Package:

**Low Inductance** - Insert molded case allows low inductance electrode designs

**Low Capacitance** - Substrate geometry optimized for reduced leakage capacitance to the base plate

**Improved Reliability** - Solder joints between power electrodes and base plate have been eliminated. Low temperature solder used to attach chips and substrate.

**Improved Manufacturability** - Soldering passes reduced from 2 to 1

**Increased Resistance to Bending Stresses** - Smaller ceramic substrates and thicker copper base minimize breakage and allow greater mounting torque
New Module Package:

Dual 300A, 1200V Trench-Gate IGBT Module
(CM300DU-24F)
Worlds Most Powerful SOP-8
CY25AAJ -8
400V, 150A
Strobe Flash IGBT

Designed for compact digital cameras

Features:
Trench gate technology
4V gate drive
High current/small package
Low $V_{CE(SAT)}$ 250V IGBT Modules
For forklift and light electric vehicles

Features:
- Low $V_{CE(SAT)}=1.1V$ ($T_j=125^\circ C, I_c=I_{C(RATED)}$)
- High Reliability Packaging
- Robust Switching SOA

<table>
<thead>
<tr>
<th>Type</th>
<th>Circuit</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM600HA-5F</td>
<td>Single</td>
<td>600A</td>
</tr>
<tr>
<td>CM450HA-5F</td>
<td>Single</td>
<td>450A</td>
</tr>
<tr>
<td>CM350DU-5F</td>
<td>Dual</td>
<td>350A</td>
</tr>
<tr>
<td>CM200TU-5F</td>
<td>Six-Pack</td>
<td>200A</td>
</tr>
</tbody>
</table>

New Product
CT60AM-18B

Features:

- Low $V_{CE(SAT)} = 2.0V$ ($T_j=125^C, I_C=I_{C(RATED)}$)
- Low tail loss
- Integrated anti-parallel diode
- TO-3PL (TO264) Outline
Conclusion

Trench-Gate technology is effective for improving the key characteristics of a wide range of power semiconductor devices.

Examples presented:

- Low voltage MOSFETs (especially small package types)
- Industrial IGBT modules (600V and 1200V)
- Special Devices (strobe flash, forklift, resonant mode)