New 1.7kV IGBT Chip with Fine Pattern and Optimized Buffer Layer

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Abstract— Since the introduction of the IGBT, improvements in power loss and efficiency have been achieved by applying new technologies. In this paper, refinements in fine pattern processing technology and optimization of the low impurity profile of the buffer layer using thin wafer technology are proposed to further reduce the power loss and improve efficiency in 1.7kV IGBT chips.

I. INTRODUCTION

Responding to widespread needs for energy conservation, IGBT (Insulated Gate Bipolar Transistor) devices are widely used in high power applications, such as inverter motor drives, uninterruptible power supplies, electric vehicles, and alternative energy. Improvement in IGBT characteristics is essential for decreasing VCE(sat) (on-state conduction loss) and ESW(off) (turn-off switching energy loss) to achieve improved efficiency. The major ways to improve IGBT characteristics are optimization of vertical carrier concentration profile by using a trench-gate structure and the reduction of the substrate thickness of LPT (Light Punch Through) devices. After many years of iterative improvements including the replacement of planar with trench gate structures, the current high performance IGBT is the CSTBTM (Carrier Stored Trench-gate Bipolar Transistor) [1-3]. This paper proposes further improvement in the CSTBTM by use of a carrier enhancement emitter structure and advanced thin wafer technology to achieve a more efficient 1.7kV IGBT.

The CSTBTM IGBT consists of a triple layered structure in the region of the trench gate, i.e., N-Emitter/P-Base/CS-layer. The CS-layer under the P-Base has the effect of reducing VCE(sat). Recently, the second generation of CSTBTM which adopts thin wafer process technology achieved a further improvement in device performance, especially by optimizing the backside collector profile on mid-high voltage region [2]. For the development of the next generation 1200V IGBT, the concept of CSTBTM(III) was proposed and developed in terms of a finer pattern for the trench gate structure and a retrograde doping profile in the CS-layer [6]. The CSTBTM(III) shows good VCE(sat)-ESW(off) trade-off relationship and large Short Circuit Safe Operating Area (SCSOA). The success of CSTBTM(III) can be attributed to the optimization of the doping distribution in the triple-layer structured emitter region of the CSTBTM and the adoption of advanced ULSI wafer process technology. In this paper, a new CSTBTM (III) at 1.7kV for which performances are further improved is proposed.

II. DEVICE STRUCTURE

Figures 1(a) and (b) show the conventional CSTBTM(II) and the new CSTBTM(III) for 1.7kV class, respectively. Table 1 compares their differences in geometry and manufacturing process. The new 1.7kV CSTBTM(III) has finer pattern process and the structure of trench gate and dummy trench partly separated. The retrograde doping profile which prevents the CS-layer from adversely affecting the MOS channel region in the middle triple layer is described in detail in [6]. Design optimization of both the arrangement of the trench gates and dummy trenches and the ratio of the trench gates to the dummy trenches was made to determine the optimum ratio. The resulting new structure has an injection enhancement effect, enhances the electron injection from N-Emitter, and accumulates the collector side carriers in the n-drift layer more than with the conventional structure. Figure 2 shows a simulation result of the hole concentration distribution of the new and conventional structure from the emitter side at on-state. In the new CSTBTM(III), the design ratio of the arrangement of the trench gates and dummy trenches is different in the type A and Type B devices. A number of comparative iterations of this nature were made to determine the optimum ratio. The resulting new structure has higher hole concentration than the conventional structure, which results in the reduction of conduction losses. As shown in Table I the wafer thickness is reduced about 24% resulting in improvement in the trade-off between VCE(sat) and ESw(off) while maintaining the wide SCSOA.

Several variations of MOS structure were evaluated, i.e., trench gate ratio versus dummy trenches in a fixed trench pitch. Particular attention was paid to the effects on gate capacitance (Cies, Coes, and Cres), Vce(sat), and Esw(off) as shown in Table II. Structure B was selected for the next generation chip after careful consideration of these factors.

III. ELECTRICAL CHARACTERISTICS

Figure 3 shows the experimental result of Vce-Ic characteristics of the new structure in comparison with the conventional structure at 125°C. The new structure is lower by 0.4V at Jc=120A/cm² than the conventional CSTBT™(III) is at Jc=100A/cm². In addition to the wafer thickness, the bulk resistivity has been optimized in the new structure to improve the trade-off relationship between Vce(sat) and Esw(off) while maintaining SCOSA (short circuit safe operating area). Figure 4 indicates the trade-off characteristics between Vce(sat) and Esw(off) of the new CSTBT™(III) at Jc=120A/cm² and CSTBT™(II) at Jc=100A/cm². In contrast to CSTBT™(II), CSTBT™(III) displays a much better trade-off characteristic. Figure 5 gives the Vce vs. Jc characteristic for the new chip at 25 and 175°C. Turn-on and turn-off waveforms are shown in Figures 6 and 7. It is particularly noted that there is no oscillation in the turn-off waveform due to optimization of the bulk resistivity and N-drift doping concentration. Figure 8 shows the waveforms at SCOSA test in the new CSTBT™(III) which has been rated at 185A. The new CSTBT™(III) exhibits wide SCOSA with more than 14µs short circuit withstand time under the test conditions of VGE=15V/-15V and VCE=1100V which provides margin over the standard 10µs specification. Key characteristics of the 1700V 6th generation CSTBT™(III) are listed in Table III.

A new diode chip was also developed to coordinate with the new CSTBT™(III) IGBT chip. Figure 9 is a photograph of the new IGBT and FWDi chips showing their relative size and physical dimensions. The forward voltage characteristic of the new diode is given in Figure 10. Reverse recovery waveforms for the new diode are shown in figure 11.

IV. PERFORMANCE ENHANCEMENT

IGBT application requirements have evolved to require a higher maximum operating junction temperature of 175°C to accommodate increased design margin, overload requirements, and elevated cooling temperatures. The new CSTBT™(III) and FWDi chips have been rated for 175°C. This increased temperature rating requires that steps be taken to offset the adverse effect it has on power cycling, particularly for the wire bonds that contact the chip itself. The new CSTBT™(III) chip utilizes a cell plug structure and an aluminum metallization process that produces a more planar surface for wire bond attachment. This gives an increased bond contact area, a stronger bond with increased peel strength, and higher reliability at the increased temperature excursion due to the 175°C junction temperature rating. Figure 12 shows the improvement in flatness of the emitter electrode surface of the new 6th generation chip. Figure 13 shows the improved peel strength of the 6th generation over the 5th generation as a function of relative ultrasonic bonding power.

V. CONCLUSION

The performance of the proposed 1.7kV CSTBT™(III) was examined by simulation and experiment. Improvement in the trade-off relationship between Vce(sat) and Esw(off) over conventional 5th generation was demonstrated while maintaining short circuit withstand capability. Applying the new carrier-enhancement emitter structure and advanced thin wafer technology, the proposed CSTBT™(III) achieves reduction in losses while meeting the 1.7kV blocking voltage class. The new CSTBT™(III) chips show great potential for improved efficiency in industrial applications of power semiconductor electronics and will be applied to 6th generation 1.7kV power modules in the near future.

REFERENCES

Figure 1: Cross section of (a) conventional CSTBT™ and (b) CSTBT™(III)

Table I: Comparison of conventional CSTBT™ and proposed CSTBT™(III)

<table>
<thead>
<tr>
<th>Item</th>
<th>CSTBT™</th>
<th>CSTBT™(III)</th>
</tr>
</thead>
<tbody>
<tr>
<td>trench pitch</td>
<td>1.00</td>
<td>0.60</td>
</tr>
<tr>
<td>wafer thickness</td>
<td>1.00</td>
<td>retro grade</td>
</tr>
<tr>
<td>cell structure</td>
<td>conventional</td>
<td>optimize p-base and dummy trench contact</td>
</tr>
<tr>
<td>emitter electrode</td>
<td>conventional</td>
<td>planarization</td>
</tr>
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</table>

Figure 2: Simulation result of hole distribution in the on state

Figure 3: Comparison of V_CE-I_C characteristics

J_C-V_CE @V_CE=15V, T_j=125 degrees C
Table II: Variation of MOS structures evaluated

<table>
<thead>
<tr>
<th>MOS structure</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
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<tbody>
<tr>
<td>Cies [nF]</td>
<td>7.1</td>
<td>5.4</td>
<td>4.4</td>
<td>3.8</td>
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<tr>
<td>Coes [nF]</td>
<td>0.25</td>
<td>0.24</td>
<td>0.25</td>
<td>0.24</td>
</tr>
<tr>
<td>Cres [nF]</td>
<td>0.07</td>
<td>0.05</td>
<td>0.04</td>
<td>0.03</td>
</tr>
<tr>
<td>V_{CE(sat)} [V] @Jc=120A/cm², Tj=125°C</td>
<td>2.49</td>
<td>2.44</td>
<td>2.36</td>
<td>2.32</td>
</tr>
<tr>
<td>E_{SW(off)} [mJ/A] @Jc=120A/cm², V_{CE}=850V, Tj=125°C</td>
<td>0.191</td>
<td>0.199</td>
<td>0.225</td>
<td>0.231</td>
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</tbody>
</table>

**Figure 4:** \( V_{CE(sat)}-E_{SW} \) trade-off comparison

**Figure 5:** VCE-JC characteristics

**Figure 6:** Turn-on waveforms
\( V_{CC}=1000V, V_{GE}=+15V/-15V, R_{GON}/R_{GOFF}=5\Omega, Tj=175°C \)

**Figure 7:** Turn-off waveforms

\( V_{CC}=1000V, V_{GE}=+15V/-15V, R_{GON}/R_{GOFF}=5\Omega, Tj=175°C \)
Table III: Characteristics of the new 1700V CSTBTM(III) chip

<table>
<thead>
<tr>
<th>Items</th>
<th>Condition</th>
<th>Typ.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>JC(sat)</td>
<td></td>
<td>120</td>
<td>A/cm²</td>
</tr>
<tr>
<td>VCE(sat)</td>
<td>Tj=125°C, Jc(sat)</td>
<td>2.35</td>
<td>V</td>
</tr>
<tr>
<td>VGE(th)</td>
<td></td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>Eoff</td>
<td>VCC=1000V, VGE=15V/-15V</td>
<td>0.25</td>
<td>mJ/pA</td>
</tr>
<tr>
<td></td>
<td>Tj=125°C, Inductive load</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>Jc(sat)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**New 1700V, 185A IGBT chip**
**New 1700V, 185A FWDi chip**

Figure 8: Short circuit test waveform

Figure 9: Photographs of the new IGBT and FWDi chips
Figure 10: $V_F$-$I_C$ characteristic at $T_j=25$ and 175°C

Figure 11: Reverse recovery waveform at VCC=1000V, $T_j=175°C$

Figure 12: Comparison of emitter electrode surface profile

Figure 13: Wire peel strength comparison vs. bond power